

What is Claimed is:

1. Digital signal processing (DSP) circuitry that independently processes a plurality of multi-channel data signals, comprising:

    a plurality of columns of registers, each said column comprising a plurality of registers arranged in serial; and

    interconnection circuitry for allowing successive channels of said plurality of multi-channel data signals to be selectively shifted through said plurality of registers each said column and to also be selectively shifted through a plurality of registers in at least one other of said plurality of columns.

2. The circuitry of claim 1, further comprising utilization circuitry for operating on data output by each said column, wherein the data signal output by each said column corresponds to the same channel.

3. The circuitry of claim 2, wherein said utilization circuitry comprises circuitry selected from the group consisting of adder circuitries, multiplier circuitries, and a combination thereof.

4. The circuitry of claim 1, wherein the interconnection circuitry comprises:

    a multiplexer circuit associated with each register in each said column.

5. The circuitry of claim 1, wherein said interconnection circuitry allows successive data

signals to be shifted to as many different said plurality of columns as needed such that the output of each of those columns is used as an input to a finite impulse response filter function.

6. The circuitry of claim 5, wherein the output of each of those columns corresponds to the same channel.

7. The circuitry of claim 1, wherein said interconnection circuitry can selectively route data signals past one or more of said registers in each said column.

8. A programmable logic device including circuitry as defined in claim 1.

9. The programmable logic device defined in claim 8 further comprising:

routing circuitry for selectively supplying signals to and receiving signals from the DSP circuitry.

10. The programmable logic device defined in claim 9 further comprising:

programmable logic circuitry connected to the routing circuitry.

11. A digital processing system comprising:  
processing circuitry;  
a memory coupled to the processing circuitry; and

a programmable logic device as defined in claim 8 coupled to the processing circuitry and the memory.

12. A printed circuit board on which is mounted a programmable logic device as defined in claim 8.

13. The printed circuit board defined in claim 12 further comprising:

a memory mounted on the printed circuit board and coupled to the programmable logic device.

14. The printed circuit board defined in claim 12 further comprising:

processing circuitry mounted on the printed circuit board and coupled to the programmable logic device.

15. A programmable logic device (PLD), comprising:

digital signal processing (DSP) circuitry that supports multiple channels of data being transmitted on the same carrier, said DSP circuitry comprising:

tap delay line circuitry that registers the data of each of the multiple channels such that the data of each channel is not mixed with the data of any other channel; and

utilization circuitry that performs a function on data received from said tap delay line circuitry.

16. The PLD of claim 15, wherein said tap delay line circuitry comprises:

at least two columns of registers, each column including at least two registers arranged in serial;

a multiplexer circuit respectively associated with a register of each said column, said multiplexer circuit operative to select one of at least two input signals being applied to said multiplexer circuit for application to said associated register, one of said input signals being one of said plurality of multi-channel signals, and another one of said input signals being the output signal of a register that is conveyed by a tap delay line from a register in a column different than the column said multiplexer circuit applies said input signal to.

17. The DSP circuitry of claim 16, wherein said associated register is a leading register in each said column.

18. The DSP circuitry of claim 16, wherein the output signal of the register being conveyed by the tap delay line is the output of a trailing register in each said column.

19. The DSP circuitry of claim 16, wherein the tap delay line conveys an output signal of a register that is being provided to a first tap to a multiplexer circuit associated with a column that provides an output signal to a second tap.

20. The DSP circuitry of claim 15, wherein said utilization circuitry selectively operates on signals output by a register in each said column.

21. The DSP circuitry of claim 16, further comprising bypass circuitry for enabling the selected input signal to be routed directly to one of said at least two registers in said column of registers.